Abstract of the Disclosure

An MOS device includes a semiconductor layer comprising a substrate of a first conductivity type and a second layer of a second conductivity type formed on at least a portion of the substrate. First and second source/drain regions of the second conductivity type are formed in the second layer proximate an upper surface of the second layer, the second layer being spaced laterally from the first source/drain region. A gate is formed above the second layer proximate the upper surface of the second layer and at least partially between the first and second source/drain regions. The MOS device further includes at least one electrically conductive trench formed in the second layer between the gate and the second source/drain region, the trench being formed proximate the upper surface of the semiconductor layer and extending substantially vertically through the second layer to the substrate. The MOS device exhibits reduced HCI effects and/or improved high-frequency performance.